

Figure 1



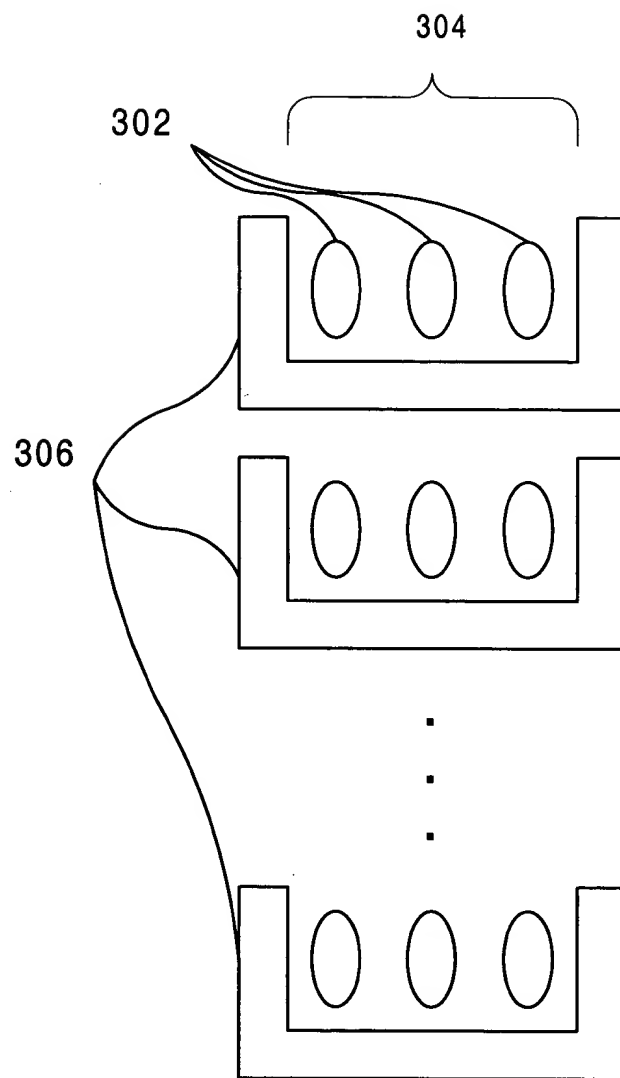


Figure 3

FIG. 4

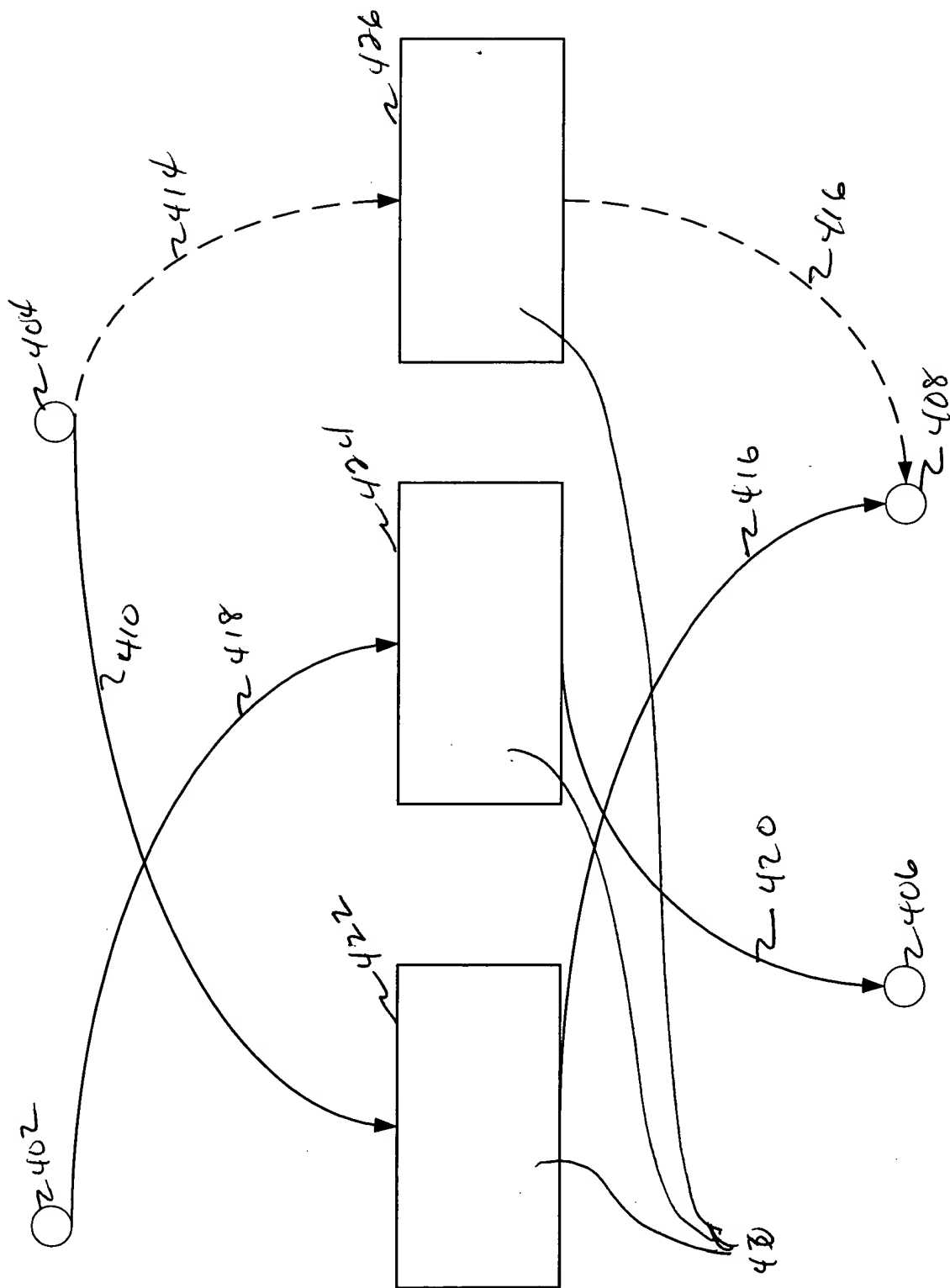


Figure 4

500

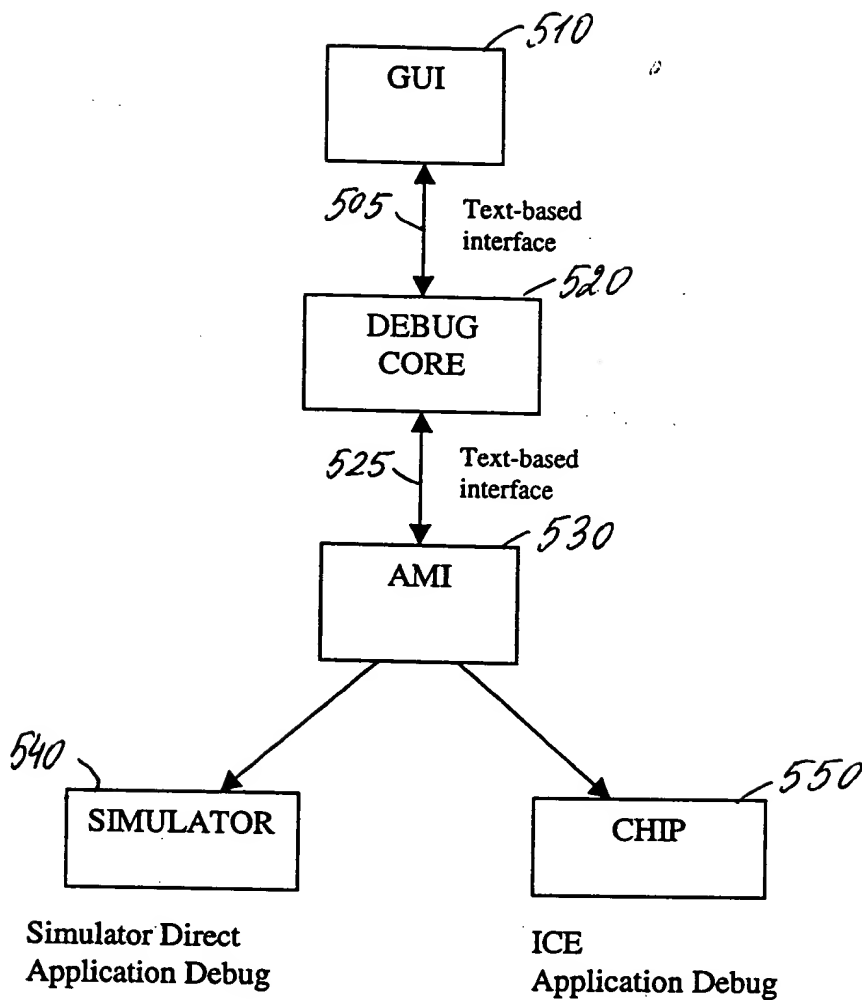


FIGURE 5A

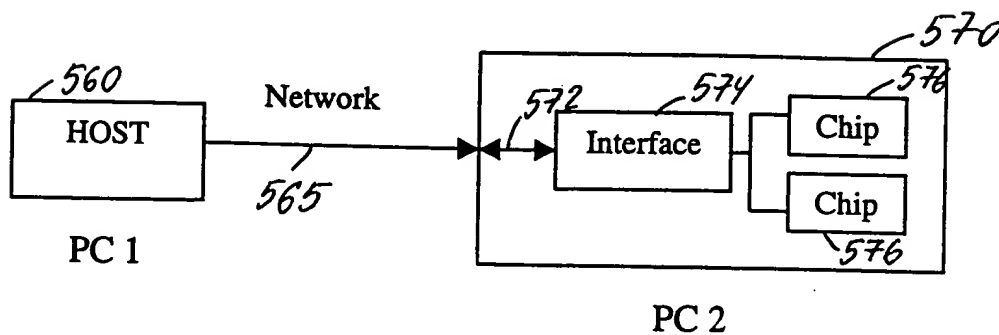


FIGURE 5B

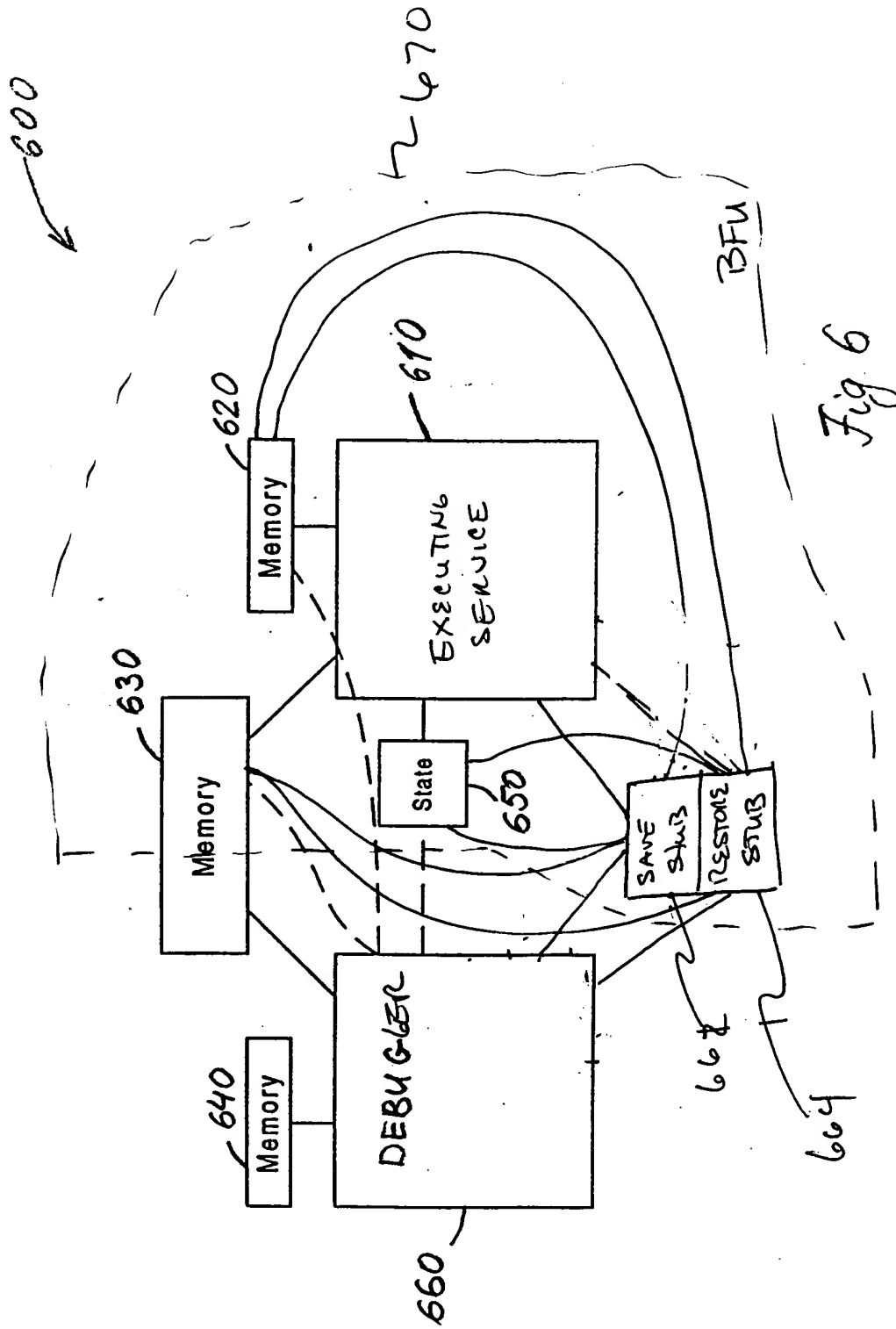


Fig 6

1	ld32 r3, (r1 + 0)
2	ld32 r4, (r1 + 4)
3	ld32 r5, (r1 + 8)
4	add r6, r3, r4

## Figure 7

1	ld32 r3, (r1 + 0)
2	ld32 r3, (r1 + 4)
3	ld32 r3, (r1 + 8)
4	ld32 r3, (r1 + 12)
5	st32 (r1 + 0), r3
6	st32 (r1 + 4), r3
7	st32 (r1 + 8), r3
8	st32 (r1 + 12), r3

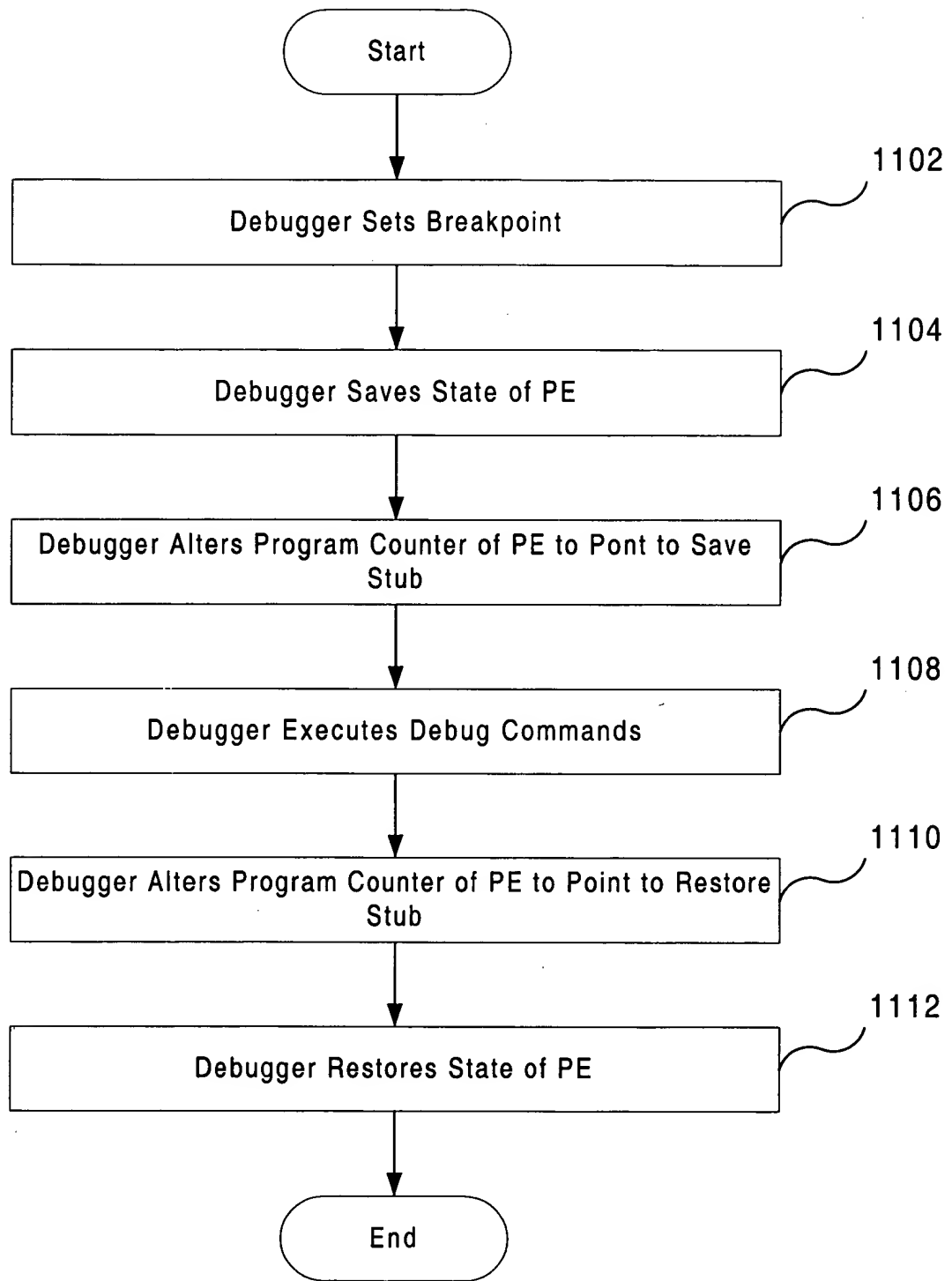
## Figure 8

1	ld32 r3, (r1 + 0)
2	ld32 r4, (r1 + 0)
3	ld32 r5, (r1 + 0)
4	ld32 r6, (r1 + 0)
5	add r7, r5, r6

## Figure 9







*Figure 11*

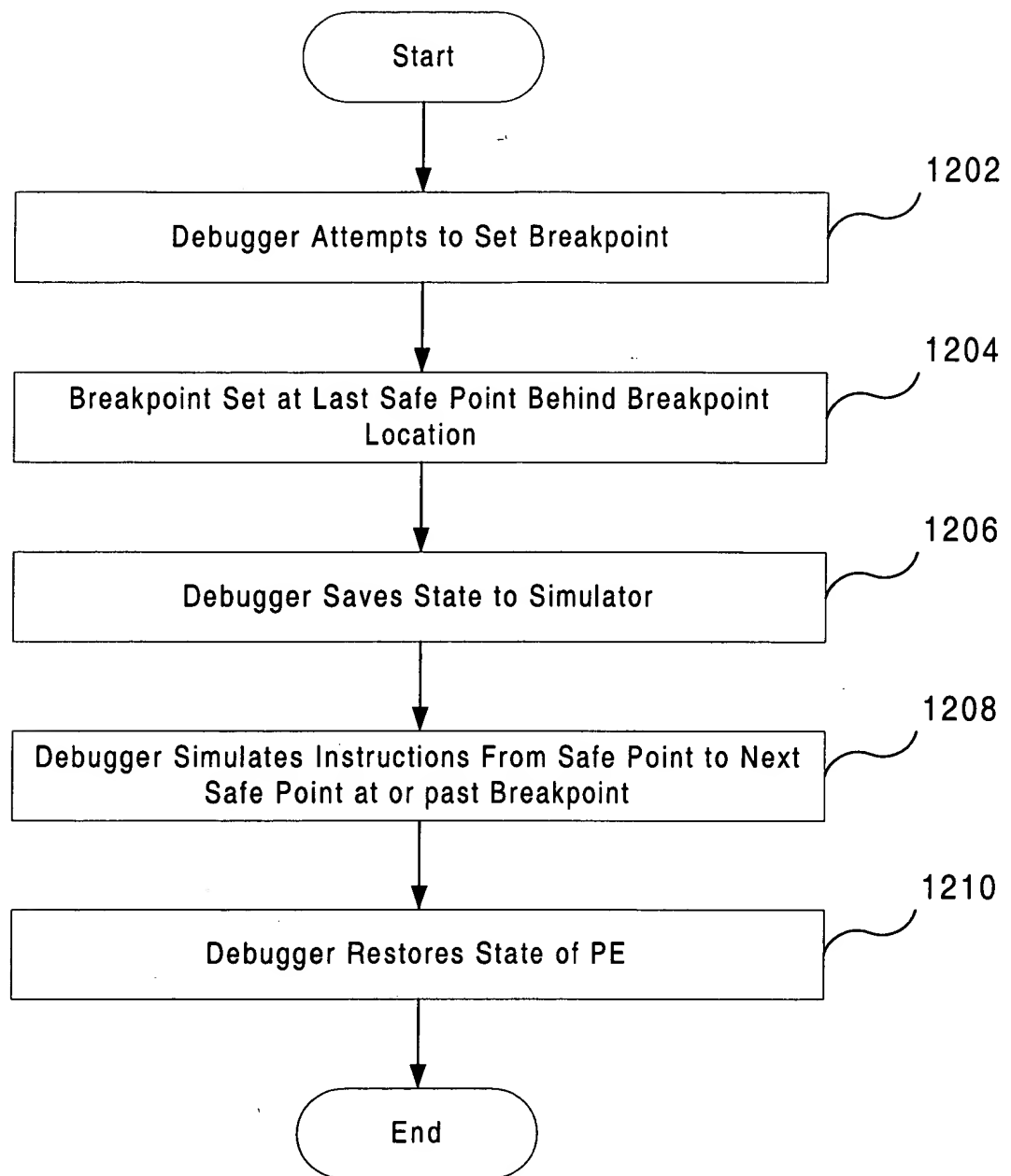


Figure 12

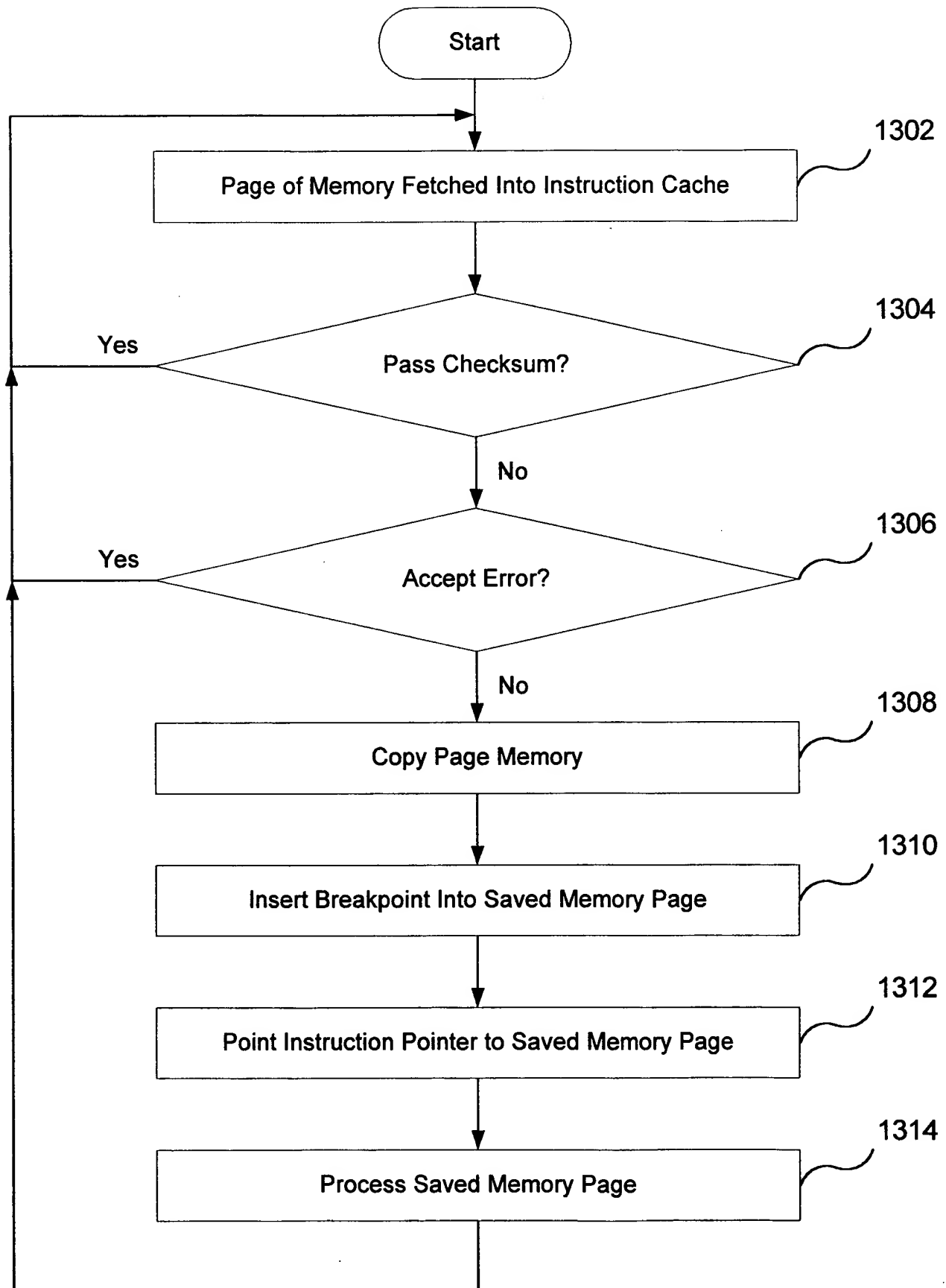


Figure 13